

List of Patents and Publications for  
Applicant's Information Disclosure Statement

APPLICANT: Bonaventure, D. et al

(Use several sheets if necessary)

FILING DATE: To be Assigned  
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## Reference Designation

## US PATENT DOCUMENTS

Examiner Initials	Document Number	Date	Name	Class/Subclass	Filing Date (If. Appro.)
I.T	AA 5,819,088	10/06/98	Reinders	395/672	03/25/93
I.T	AB 6,212,512	04/03/01	Barney, et al.	707/1	01/06/99
I.T	AC 6,260,190	07/10/01	Ju	717/7	08/11/98

## FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class/Subclass	Translation Yes No
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## OTHER ART (Including Author, Title, Data, Pertinent Pages, etc.)

I.T	AD	Cheng, W. et al. "Code Generation of Nested Loops for DSP Processors with Heterogeneous Registers and Structural Pipelining" ACM Transactions on Design Automation of Electronic Systems, Vol. 4, No. 3, July 1999, pp 231-256
I.T	AE	Eichenberger, A. et al. "Optimum Modulo Schedules for Minimum Register Requirements", ACM 0-89791-726/6/95/0007, pp 31-40, 1995
I.T	AF	Chekuri, C. et al. "Profile-Driven Instruction Level Parallel Scheduling with Application to Super Blocks", IEEE, 1072-4451, 1996
I.T	AH	Shieh, J. J. et al. "On Reordering Instruction Streams for Pipelined Computers", 22 <sup>nd</sup> Annual International Workshop on Microprogramming and Microarchitecture, August, 1989
I.T	AI	Shieh, J. J. et al. "Fine Grain Mapping Strategy For Multiprocessor Systems", IEEE Proceedings, Volume 138, Number 3, May, 1991
I.T	AJ	Kim, B. M. et al. "Resource Allocation and Code Generation For Pointer Based Pipelined DSP Multiprocessors", IEEE, 1990
I.T	AK	Aizikovitz, NE. et al. "Limiting Lifetimes of Register Sequences to Improve Register Allocation" TDB, Vol. 38, No. 11, pp 89-92

Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.